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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,675	06/22/2005	Helge Betzinger	A36433 PCTUSA 066340.0125	6649

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EXAMINER	
TSENG, CHENG YUAN	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/516,675	BETZINGER ET AL.	
	Examiner	Art Unit	
	Cheng-Yuan Tseng	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *December 3 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/7/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/516,675 has a total of six claims pending in the applications; there are one independent claim and five depending claims. Claims 1-7 were canceled in preliminary amendment filed on December 12th, 2004. At the same time, claims 8-13 were added.

2. The specification and the claims have been examined with the results that follow.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Preliminary Amendment

4. The applicant's preliminary amendment has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.115.

5. The applicant's submissions of preliminary amendment dated December 3, 2004 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending.

Information Disclosure Statement

6. As required by M.P.E.P. 609(C), the applicant's submissions of the Information Disclosure Statements dated July 7th, 2005 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

7. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. As required by M.P.E.P. 201.14(c), acknowledgement is made of applicant's claim for priority based on its PCT applications filed on December 5 2003 (PCT/DE/03/01748) and its German application filed on June 5th, 2002 (DE 102 25 099.5).

Specification

8. The abstract of the disclosure is objected to because it contains more than 150 words. Correction is required. See MPEP § 608.01(b) and 37 CFR 1.72(b).

(b) A brief abstract of the technical disclosure in the specification must commence on a separate sheet, preferably following the claims, under the heading "Abstract" or "Abstract of the Disclosure." The sheet or sheets presenting the abstract may not include other parts of the application or other material. The abstract in an application filed under 35 U.S.C. 111 may not exceed 150 words in length. The purpose of the abstract is to enable the United States Patent and Trademark Office and the public generally to determine quickly from a cursory inspection the nature and gist of the technical disclosure.

9. The disclosure is objected to because of the following informalities:
   a. In page 1, second line from last paragraph, the "(very Long Instruction Word)" should be "(Very Long Instruction Word)".
   b. In page 5, line 15, consider remove "a" from "combining a plurality of FIWs".
   c. In page 6, line 16, consider revise "providing the a structured supports".
   d. In page 10-11, the reference numerals for figures are incorrect from 7-27.
   e. In page 12, line 6, correct the "container 11;12." The semicolon should be comma.
   f. In page 12, line 17, correct "that are are taken from the first and second".
   g. In page 5, line 6, the specification uses "Command Code Mode" to refer one of its operation mode. Such an operation mode is understood as VLIW mode in the art. Consider revise with conventional term. See MPEP 608.01(g).
   h. In page 6, line 19, the specification uses "Reference Instruction Mode" for one of its operation mode. Such an operation mode is understood as SIMD in the art. Consider revise with conventional term. See MPEP 608.01(g).

Appropriate correction is required.

Claim Objections

10. Claims 9-13 are objected to because of the following informalities:

    a. In claim 9, 10, 11, and 13, the "The method of claim 1", should be revised as "The method of claim 8".

    b. In claim 12, the "The method of claim 4", should be revised as "The method of claim 11".

    c. In claim 8, the full name of acronym VLIW, TVLIW, HVLIW, and FU need to be supplied on first use.

    d. In claim 8, line 19, consider revise as "the respective ~~available~~ TVLIW".

    e. In claim 8, line 14-15, consider revise "~~The~~ [a] first and ~~the~~ [a] second FU".

    f. In claim 9, consider revise "for constructing the VLIW ~~(22)~~".

    Appropriate correction is required.

Claim Rejections - 35 USC § 101

11. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 8-13 are rejected under 35 U.S.C. §101, because the claimed invention is directed to non-statutory subject matter.

13. The claimed subject matter lacks a practical application of a judicial exception (abstract idea, law of nature, or natural phenomena), since it fails to produce a useful, concrete and tangible result. See M.P.E.P. 2106 II. For a judicial exception (such as abstract idea or functional descriptive material, e.g., code or computer program instructions is) to be eligible for patent protection, the claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373-74, 47 USPQ2d at 1601-02. For produced result to be a tangible result, it must be more than just a thought or a computation. Instead, it must

have real world value rather than being an abstract result. More specifically, the claimed subject matter is too preliminary to produce any tangible result that accomplishes a practical application.

14. As per claims 8-13, first, in claim 8, the instant application claimed "HVLIW converted from TVLIW in the configuration phase". The claim language of the last (second) step suggests making such a product formulated; however it doesn't suggest bring the result into existence for use or being used immediately as it has produced tangible result. Such an invention claim is known as nonstatutory subject matter, under judicial exception. See M.P.E.P. 2106 IV.

15. Second, in claim 8, the preamble addressed "a method for actuating function units", however nowhere in the rest of the claim describes actuating process other than prepare instructions for actuating to function units. Such a claim doesn't accomplish the stated purposes given in the preamble. Therefore, it is not produce a useful, concrete, and tangible result.

Claim Rejections - 35 USC § 102

16. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 8-13 rejected under 35 U.S.C. 102(b) as being anticipated by Pechanek et al. (U.S. Patent 6,101,592).

18. As per claim 8, Pechanek et al. discloses a method for actuating function units in a processor [fig. 1A, processor 100], wherein a configuration phase [fig. 4A, translation process 400] involves a series of primary instruction words [fig. 4A, 15-bit compacted-1 instruction 401] that come from a translation of a program code being divided into a

series of instruction word parts [fig. 4A, 32-bit ADD instruction 403], with a program cycle involving instruction words which actuate [col. 3, lines 43-46, and fig. 1A, 1B, the compact instruction is "instruction words" in which, with operating codes, they active each PE's ALU in the processor 100] the processor being constructed in the full instruction word length to form a VLIW [fig. 5, VLIW is instruction of store+load+alu instructions+mau instruction+dsu instructions] and being buffer-stored in an instruction word memory (cache) [fig. 5, VIM], the method comprising:

a. a first step that involves a primary instruction word [fig. 4A, 15-bit compacted-1 instruction 401] being divided, in the configuration phase [fig. 4A, ALU translation process 400], into the series of a particular number of instruction word parts [fig. 4A, 32-bit ADD instruction 403] which are used for constructing a respective VLIW [fig. 5, VLIW is instruction of store+load+alu instructions+mau instruction+dsu instructions,or fig. 1A, instruction native to SP/PE0, PE1, PE2, and PE3] during the execution phase, with a respective first and second FIW (Function Instruction Word part) [fig. 6, first FIW is bits 29-15, second is bits 14-0],

b. being preceded [fig. 6D, Translation Process 670, 680] with an associated first or second operating code [fig. 3A, bits 27-24 is opcode], which thus determines [fig. 6D, VIMOffs in (657, 655)] how the cache's memory location taken up [fig. 7A, VIM Load/Store Control coupled to iVIM Memory VIM as cache] by the respective FIW is handled in the execution phase [fig. 8, execute units (840, 842, 844, 846, 848)],

c. wherein the respective first and second operating code [fig. 3A, bits 24-27] are respectively followed by an associated first and second tag [fig. 3A, bits 28-29] that represent the information regarding which of the first and the second FU [fig. 3A, bits 24-27] actuates [col. 3, lines 43-46, and fig. 1A, 1B, the compact instruction is "instruction words" in which, with operating codes, they active each PE's ALU in the processor 100] the respective FIW [col. 3, lines 43-46, and fig. 1A, 1B],

d. wherein, the respective first and second operating code [fig. 3A, bits 24-27] and their associated first or second tag [fig. 3A, bits 28-29] are combined [fig. 2-5, instructions and tags are combined] with the respective first and second FIWs to form the first and second TVLIW [fig. 5, Compacted-1 Instructions] containers all of which represent the TVLIW; and

e. TVLIW being converted into an HVLIW [col. 17, claim 6, HVLIW is the Task Specific Instruction] in the configuration phase [col. 11, line 63, VIM Translation Compacted Type-2 Instructions], wherein the HVLIW contains a preceding general header [fig. 1B, header (17, 15, 13, or 11)], and wherein the HVLIW with its code-compressed structure [fig. 5, Store Unit Instructions, Load Unit Instructions, MAU Instructions, DSU Instructions] replaces all functions of the TVLIW.

19. As per claim 9, Pechanek et al. discloses a Command Code mode of operation of the HVLIW and its associated general header is implemented so that the general header [fig. 2B, bits 30, 31 of the instruction] is followed directly by the first and second FIWs [fig. 2B, bits 28, 29 and bits 13, 14 for the first and second FIWs] required for constructing the VLIW,

a. wherein the general header stores the information in coded form [col. 8, lines 30-44, bits 28, 29, 13, 14], which indicates all combinations regarding which of the first and second FIW (instruction word part) is provided, after decoding in the execution phase for actuating [fig. 3A, Each coded form also has its corresponding functional unit (FU) in the execution unit.] a respective first and/or second FU (function unit) in the processor [fig. 3A, 3B, 3C and 3D]

b. wherein the general header stores which first and/or second FIW take up memory locations in a cache [fig. 6B, the VIM (cache) memory are defined to be accessed with bits 26-24 (as well as 11-9)] and whether or which operations are to be executed with the respective memory content in the execution phase in the cache when constructing the VLIW.

20. As per claim 10, Pechanek et al. discloses "a first part of the general header is provided with a header mode that contains information about the Command Code mode of operation of the HVLIW and of the general header,
    a. wherein the first part is followed by a second part that stores, coded as table values [fig. 6B, bits 27-29 (as well as bits 12-14)], the respective most needed combination regarding which of the respective [fig. 6B, The operating code encoding scheme will determine the actuated functional unit (FU) at execution time.] FUs is actuated by which of the first and second FIW" as in [FIG 6B drawing].
    b. a third part is connected as CE information [fig. 6B, bits 24-26] and contains a pointer which refers to a provided location in a dictionary, and
    c. wherein the last part of the general header provided is the supplementary information." as in [FIG 6B drawing, and col. 13, lines 43-46].

21. As per claim 11, Pechanek et al. discloses a 'reference instruction' mode [fig. 7B] of operation of the HVLIW and of the contained general header is implemented in which the FIWs provided for constructing the VLIW in the execution phase are buffer-stored [fig. 7B, bits 17-15 (UnitVIM) for the use of buffer-stored cache] in the cache, wherein the associated header mode bears a correspondingly decodable tag [fig. 7B, bits 28-25 (CtrlOp) as a type of instruction opcode field is the "decodable tag"] for this 'reference instruction' mode of operation,
    a. Wherein the "reference instruction" mode [fig. 6B, Group bits (bits 31-29) + Instruction bit-23 to make such HVLIW specific to the 'reference instruction' mode] of operation [fig. 7] is initiated by a specific HVLIW that contains an address statement [col. 14, lines 16-18] which is used to refer to a reference instruction,
    b. the subsequent HVLIW which likewise bears the tag for the 'reference instruction' mode of operation, contains a relative address for the address statement provided by the reference [col. 14, lines 18-24, Bits 18-21 specify that up to 16 instructions are to be loaded in the specific functional unit's VIM,

indicated by bits 15-17. The instructions begin loading at the address generated by the addition of an address value located in one of two Vb registers, selected by bit-9, plus the VIMOFFS offset address, bits 0-7. The prior art shows the InstrCnt (Bits 18-21) as a tag for counting subsequent HVLIW instructions, and the Vb registers can hold addresses.]

c. a mask appended to it for the FUs which are to be excluded from the actuation. [col. 14, lines 56-59, The five state d-bits 821, 823, 825, 827, and 829 are LV-loaded disable bits for the instruction slots that indicate either: the instruction slot is available-for-execution or it is not-available-for-execution. The d-bits in the prior art anticipate the "mask" for the functional units (FU) utilizations.]

22. As per claim 12, Pechanek et al. discloses the address statement of the specific HVLIW which initiates the 'reference instruction' mode of operation refers to a general address [Instruction bit-23 that specifies if at least one instruction is to be loaded or if the disable d-bit for the specific address is to be loaded. (Column 14, lines 16-18)]. The Instruction bit-23 in prior art can specify if a general (or particular) address needs to be loaded as "address statement" in the instant application.

23. As per claim 13, Pechanek et al. discloses the execution phase involves the HVLIW being decoded in a decoder which is equipped with a header decoder, a CMDT, a cache and a cache miss repair logic unit, wherein the HVLIW is buffer-stored in the cache, and wherein the header decoder identifies the mode of operation of the general header from the header mode stored therein [col. 10, lines 58-63, In Fig. 4A, there are three translate blocks 409, 411, and 413, which allow simple fixed translations to a known state for a given instruction mapping. For example, the group code bits 30 and 31 for the dual compacted instructions 415 are 00, which enable the translation process logic 400. The Translate block 400 which decode group code bits and Translate block (409) are analogous to the claimed "header decoded". The Translate block (411) which decodes operating codes (opcode), and Translate (413) are analogous to the CMDT, and the VIM (109 in figure 1), which anticipates cache and cache, miss repair logic. It is inherently

known in the art that the cache has coherency phenomena where a cache replacement (as cache repair) is always exist.]

a. wherein the identified header mode is taken as a basis for decompressing [col. 10, lines 60-62] the values of the FU-C information which are provided in the general header by means of a comparison with the CMDT and in conjunction with the CE information which is likewise taken from the general header [fig. 4A, 4B, The translate (409, 411, 413, 432) anticipates information translation of the CE, CMDT, and FU-C.],

b. wherein the identified header mode is taken as a basis for processing the supplementary information [col. 10, lines 60-62, The prior art uses examples of the group code bits (which anticipates header mode) to demonstrate the translation process will vary based on its information.] in the general header,

c. wherein possible incorrect access [fig. 1, The VIM (109) which anticipates cache and cache miss repair logic. It is inherently known in the art that the cache has coherency phenomena where a cache replacement (as cache repair) is always exist. After a necessary cache miss recovery, a valid data will be provided at the cache output as result.] during buffer-storage in the cache (cache miss) is remedied by the execution of an error handling routine in a cache miss repair logic unit and a valid VLIW is provided at the output of the decoder.

Conclusion

24. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

25. Per the instant office action, claims 8-13 have received rejection in the first action on the merits and are subject of a first action non-final.

26. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See M.P.E.P 707.05(c).

27. The following references teach processor method and apparatus for instruction set architecture with dynamic compact instructions.

    U.S. Patent Number

    - 6,101,592
    - 7,080,235

    Non-patent literature

    - Markus et al. Optimized Address Assignment for DSPs with SIMD Memory Access, IEEE, 2001
    - Weiss et al. Dynamic Codewidth Reduction for VLIW Instruction Set Architectures in Digital Signal Processors

28. The examiner requests, in response to this office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

29. When responding to this office action, applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

    In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheng-Yuan Tseng whose telephone number is 571-272-9772. The examiner can normally be reached on 08:00-17:00 Monday-Thursday.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 2, 2007

Cheng-Yuan Tseng
Patent Examiner
Art Unit 2183